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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/538,911
Filing Date: June 14, 2005
Appellant(s): FRIED ET AL.

Steven Capella
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/04/2008 appealing from the Office action mailed 09/18/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5512517	Bryant	04-1996
6960606	Bryant et al.	6-2001
2002/0135041	Kunikiyo	9-2002
6770516	Wu et al.	9-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-9, 11, and 13 are rejected under 35 U.S.C. 102(b) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996).

As to claim 1, Bryant discloses a method (See Figs. 6A-9) for forming a spacer (I-poly spacer 22; Fig. 8C; column 4, line 53) for a first structure (Gate poly 28 and sidewall portions of Cap Ox 30; Fig. 8C; column 4, line 64 and column 5, line 2) and a spacer for at most a portion of a second structure (Cap

Ox 30 and the tip top of Gate poly 28; Fig. 8C; column 5, line 2, and column 4, line 64), the method comprising the steps of:

depositing a first material (poly of Gate poly 28; Fig. 8C; column 4, line 64);

forming a second material (oxide of Cap Ox layer 30, notably this being the material of film 32 as well; Fig. 8C and in 7B-C and 8B-C for 32 being the same material; column 5, line 2) over the first material 28;

forming the first structure (Gate poly 28 and sidewall portions of Cap Ox 30; Fig. 8C; column 4, line 64, and column 5, line 2) from the first and second materials;

making the second material 30/32 overhang the first material 28;

and forming a spacer (I-poly spacer 22; Fig. 8C; column 4, line 53) under the overhang (overhang of the portion of the oxide designated as 33; Fig. 8C). (Notably, this final step does not necessarily imply order, but even if it did then this is accounted for by I-poly 22 taking a final spacer form under the overhang portions above it as the RIE works through the respective materials).

As to claim 2, Bryant further shows the method of claim 1, wherein the second structure (Cap Ox 30 and the tip top of Gate poly 28; Fig. 8C; column 5, line 2, and column 4, line 64) is made of monocrystalline silicon (all layers of polycrystalline silicon such as the tip top of Gate poly contain inherently portions of monocrystalline silicon), and the first material is made of polycrystalline silicon (Gate poly 28, Fig. 8C; column 4, line 64).

As to claim 3, Bryant further shows the method of claim 1, wherein the second material 30/32 is formed such that the second material has a faster oxidation rate (the oxide 30 would grow oxide faster than the lower portions of poly 28 far below it if the device subjected to oxygen since the poly far below it is surrounded by oxide and more poly than the upper portion of poly 28 feeding the oxide layer 30) the first material (lower parts of gate poly 28).

As to claim 6, Bryant further shows the method of claim 3, wherein the step of making includes oxidation (making oxide) to form the overhang as a result of a differential oxidation rate (oxide spacer film 32 deposited on cap ox 30 will grow faster than any oxide on the lower portion of gate poly 28) of the second material with respect to the first material (Also, in the alternative, a slight oxide film will develop on Cap ox 30 faster than it will inherently grow on the lower portion of gate poly 28 in the ambient atmosphere of the processing chamber which will be oxidation occurring to form an overhang resulting from the difference in oxidation rates between the first and second materials).

As to claim 7, Bryant further shows the method of claim 3, wherein the step of making includes forming oxide on sides of the first structure and the second structure (portions of cap ox 30 formed on the sides of poly gate 28; Fig. 8C).

As to claim 8, Bryant further shows the method of claim 1 (with the alteration of referring to PSG layer 44 as "the second material"; Fig. 10C; column

5, line 33), wherein the second material 44 has different thermal reflow properties than the first material (Gate poly 28, Fig. 8C; column 4, line 64).

As to claim 9, Bryant further shows the method of claim 8, wherein the second material is one of BPSG and PSG (PSG layer 44; Fig. 10C; column 5, line 33).

As to claim 11, Bryant further shows the method of claim 1, wherein the step of forming the spacer 22 includes:

depositing a spacer material 22; and directionally etching (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) to form the spacer material 22 away except under the overhang.

As to claim 13, Bryant further shows the method of claim 1, wherein the first structure is a gate (gate poly 28 portion of the first structure in claim 1 above) and the second structure is a fin (a protruding portion of a mechanism resembling a fin) of a FinFET (The structure is a FET and it has a fin, broadly interpreted it is a finFET).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-5, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Bryant et al. (US 6,960,806, filed 06/21/2001).

As to claims 4 and 5, Bryant discloses the method cited above for claim 3. However, regarding claim 4, Bryant fails to disclose a method as cited above for claim 3, wherein the second material includes a dopant including at least one of the group comprising: Arsenic, Germanium, Cesium, Argon, and Fluorine. Regarding claim 5, Bryant also fails to disclose a method as cited above for claim 3, wherein the second material is a deposited polycrystalline silicon-germanium alloy.

In the same field of endeavor, Bryant et al. show a method of forming a FinFET with a second material as part of the top portion of the gate made from doped polysilicon (poly 218; Fig. 5; column 4, line 51) which can include Si-Ge (technology Si-Ge being used to make the poly gate; column 11, line 38) made using arsenic implants (n-FETs need to be implanted using arsenic; column 10, line 21).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of making an n-doped polysilicon-Ge for an upper layer of a gate as taught in Bryant et al. to have made the upper portion of the poly gate in Bryant with the motivation of using a material which has a greater number of carriers and a greater carrier mobility than ordinary polysilicon as used in Bryant (dopants increases the numbers of

carriers, and SiGe's bandgap structure results in higher carrier mobility, See US 5,461,250, dated 08/10/1992, column 1, lines 50-51). The reasonable expectation for success results from the polysilicon-Ge gate structures as taught in Bryant et al. being well known in the art to form better gates for FET's such as in Bryant.

Regarding claim 14, Bryant discloses a method for forming a gate structure (Gate poly 28, Fig. 8C; column 4, line 64) and associated spacer (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B; column 5, line 22) for a FET, the method comprising the steps of:

depositing a first gate material (poly 28, Fig. 8C; Column 4, line 64) over a portion of the FET;

forming a second material (top portion of Gate poly 28, Fig. 8C; column 4, line 64) over the gate material 28, wherein the second material 30 has a faster oxidation rate (the top portion of Gate poly 28 will grow oxide faster than the lower portions of the poly gate material due to increased exposure) than the gate material;

forming the gate structure (Gate poly 28, Fig. 8C; column 4, line 64) into (interpreted as being "from" as listed in objections) the gate material 28 and the second material 30/32;

oxidizing (growing oxide layer 32; Fig. 7C; column 5, line 10) to cause the second material 30/32 to overhang the gate material 28;

and forming a spacer (I-poly layer 22 is subjected to RIE to form spacers; Fig. 8B or 8C; column 5, line 22) under the overhang.

Regarding claim 15, Bryant discloses a method cited above for claim 14, wherein the gate material 28 is polycrystalline silicon (Gate poly 28, Fig. 8C; column 4, line 64).

Regarding claim 16, Bryant discloses a method cited above for claim 14, wherein the second material is a polycrystalline silicon (top portion of Gate poly 28, Fig. 8C; column 4, line 64) formed such that the second material has a faster oxidation rate than the first material (top portion of Gate poly 28 will oxidize faster than the lower portion due to increased exposure).

Regarding claim 17, Bryant discloses a method cited above for claim 14, wherein the step of oxidizing (forming oxide 32; Fig. 6B; column 5, lines10-11) also forms oxide on sides of the gate 28.

Regarding claim 18, Bryant discloses a method cited above for claim 14, wherein the step of forming the spacer includes:

depositing a spacer material 22; and

etching (I-poly layer subjected to RIE to form spacers; Fig. 8B; column 5, lines 22-23) the spacer 22 material away except under the overhang.

However, regarding claims 14-18, Bryant fails to disclose a method for forming a finFET wherein a monocrystalline fin extends through the lower portion, and has a spacer surrounding its fin, as opposed to a FET which lacks these features due to the nature of the particular design of FET illustrated.

In the same field of endeavor, Bryant et al. teach a method of forming a finFET wherein a monocrystalline fin (poly fin 218 including small portions of monocrystalline Si as all poly inherently does; Fig. 5; column 4, line 51) that has a spacer (spacer 244; Fig. 14; column 7, lines 29-30) partially surrounding its fin 218.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming a finFET wherein a fin that has a spacer partially surrounding its fin as taught by Bryant et al. to have formed the FET made in Bryant with the motivation of utilizing the standardized finFET design and gaining the benefits in terms of gate control that finFET gate wrapped around a channel offers.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Kunikiyo (US Pub. 200210135041, dated 0912612002).

As to claim 10, Bryant shows a method of forming an FET as cited above for claim 9.

However, Bryant fails to disclose a method wherein the method of forming an overhanging portion from a PSG containing material includes heating the material and causing it to reflow to form an overhanging portion.

In the same field of endeavor, Kunikiyo teaches a method of forming an overhanging (overhang; page 7, [0112], line 3) portion from a PSG (BPSG; page

7, [0112], line 1) containing material by heating the material and causing it to reflow (reflow; page 7, [0112], line 2).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming an overhang portion from BPSG as taught in Kunikiyo to have made the overhang portion in Bryant, with the motivation that BPSG should be used for overhang (BPSG should be used for overhang; page 7, [0112], line 3).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant (US 5,512,517, dated 04/30/1996), in further view of Wu et al. (US 6,770, 516, filed 09/05/2002).

As to claim 12, Bryant shows a method of forming an FET as cited above for claim 11.

However, Bryant fails to disclose a method wherein the spacer material is at least one of silicon nitride and (read as "or" as in objections above) silicon oxide.

In the same field of endeavor, Wu et al. teach a method of forming spacers (spacer 9; Fig. 5B; column 4, line 7) from silicon nitride (silicon nitride spacers 9; Fig. 5B; column 4i line 7).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have used the method of forming spacers out of silicon nitride as taught in Wu et al. to form the spacers in Bryant, with the

motivation that in order to form N and P type source/drain regions in undoped portions of silicon shapes a silicon nitride spacer has to be employed (to form N and P type regions in silicon, a silicon nitride spacer has to be employed; columns 3 and 4, lines 66-67 and 1-3).

(10) Response to Argument

Applicant's arguments, see Brief, filed 04/04/2008, include three major arguments and arguments to dependents based thereon.

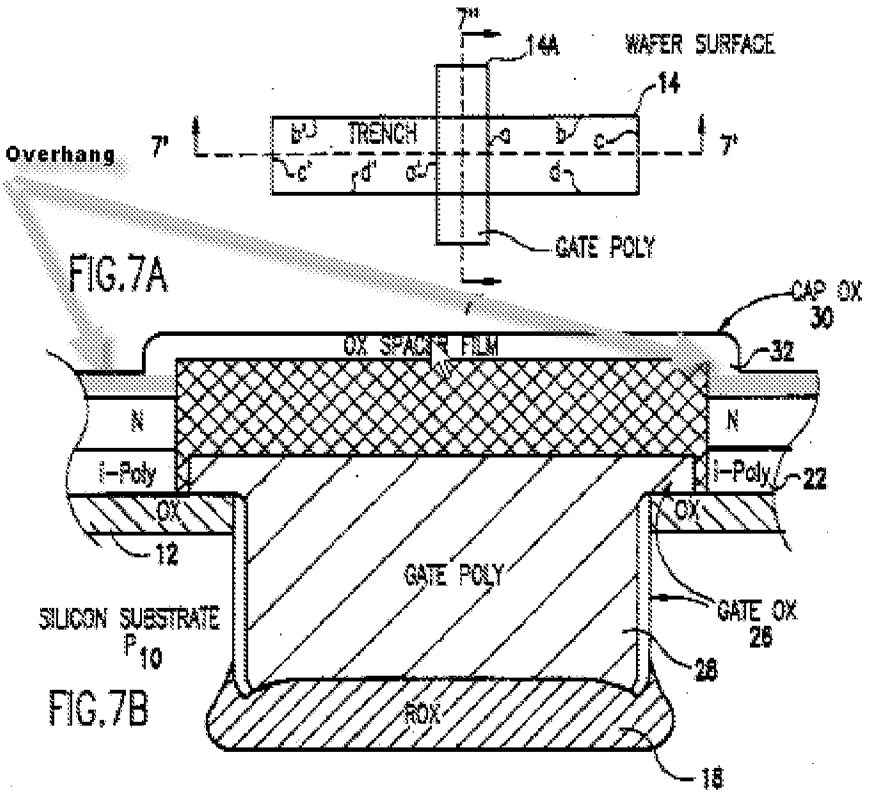
1. In regard to all of the claims that since Bryant discloses forming a spacer material 22 first, before formation of a material of a cap oxide 30 and later the deposition of ox spacer film 32 it is not apparent to the applicant how Bryant can be said to anticipate forming a spacer under an overhanging structure as required by the present claims since no overhanging structure exists at the time the spacer is formed in Bryant.

2. That an alternative rejection to claim 6 citing inherency regarding limitations of claim 6 is not well founded due to the nature of the formation of layer 32 as a deposited coating. This appears to be a misunderstanding of the rejection in as much as there are two separate statements of rejection being put forth as alternative rejections to claim 6. One is the oxidizing deposition of layer 32 is oxidizing the surface of the underlying layers at a rate faster than it is oxidizing any portions of any of the underlying layers below the surface. And the second, alternative view, is that the poly layer 22 will be oxidized somewhat by oxygen in the CVD ambient during deposition inherently, and that

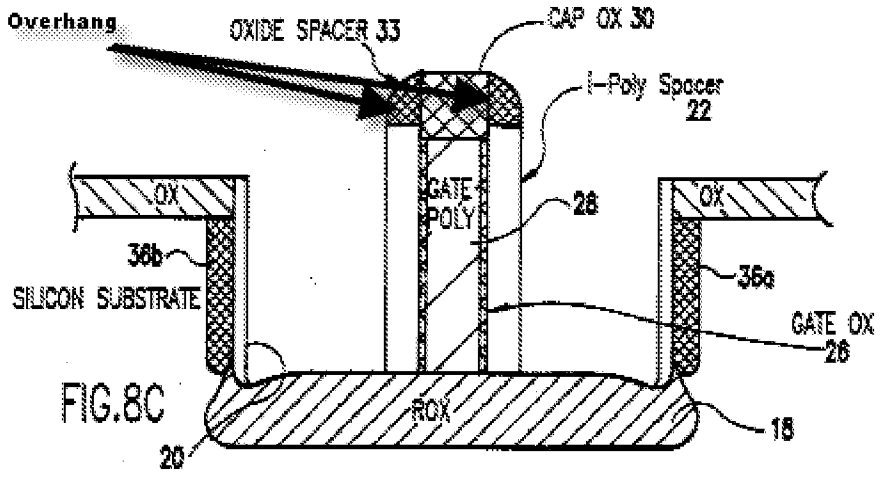
more oxidation will occur at the upper portions of 22 than at the lower portions of 22, in all oxidation processes, and in most oxidation processes this happens even more so due to the nature of oxygen diffusing through poly diminishing the amount that is able to reach lower regions in most oxidation procedures. It appears the applicant has only argued the second, alternative, view of the grounds of rejection and thus the first view stands uncontested.

3. In regard to claim 10 that since Bryant does not disclose an overhang in the above argument and it also does not disclose a trench then it is not apparent how Kunikiyo would lead one to form an overhang by reflow in Bryant.

It is the examiners position that the end “spacer” embodiment of the material which I-poly spacer 22 is made from is indeed “formed under the overhang" (See Fig. 8C and more fully taking into account the three dimensional form of the structure depicted in Fig. 7A-C and 8A-C). With the overhang being created by the material of cap ox 30 silicon dioxide, which ox spacer film 32 (and subsequently ox spacer 33) are also formed of, creating an overhang. This overhang can be viewed in no less than the following depictions as it is persistently overhanging over top of the material that spacer 22 is formed from throughout several steps.



Then the overhang becomes this overhang as RIE goes through layer 32:



Subsequently RIE completes the etch through the material spacer 22 is formed from.

Further, the examiner understands from the wording of claim 1 that there is to be no particular sequence or order implied by the last two lines. Though, even if there were, that is accounted for by the rejection in as much as the final form of spacer material 22 in Fig. 8C is clearly the formation of a spacer under the overhang of second material silicon dioxide formation 33 as in the depiction above this paragraph. Thus it has been shown that all claim limitations of claim 1 have been met by Bryant.

As to the inherency statement in claim 6, so far as the examiner is aware, known techniques of oxidizing silicon in a conformal fashion involve oxygen atoms near the surface of silicon as in Bryant. It is also known that even at ambient temperatures oxygen near the surface of silicon will form a thermal oxide layer. This effect may be controlled to acceptable levels in processes and depending on the dimensions of the device being created this effect may be more or less noticeable, but it will still occur, and there will be a difference in the oxidation rate of a poly layer and a silicon oxide layer resulting in a difference in the overall oxide layers created thereon. What is more, in this situation the discussion is involving a portion of the poly layer designated by the examiner below the surface of the poly layer which one would be very hard pressed to oxidize at a rate anywhere near the oxidation rate of the existing silicon oxide on the top of the device, thus a large differential rate exists. In any event, this is merely an alternative way of viewing the situation, only to be considered if the first alternative in the rejection should be overcome. The applicant has made no attempt to argue the first stated rejection of claim 6 thus the claim will stand rejected at least on those grounds even if the alternative view of the grounds of rejection should be decided to be incorrect.

Bryant et al. (6,960,806) is not relied upon to show an overhang, as one is already present in Bryant (5,512,517), and thus claims 4-5, and 14-21 stand rejected as in the prior Office Action.

As to claim 10 Kunikiyo is not relied upon to show an overhang, as one is already present in Bryant, and thus claim 10 stands rejected as in the prior Office Action and additionally a trench is shown in Bryant in Fig. 8C though the examiner cannot even find a limitation requiring a trench in claim 10 or any claims from which it depends, thus there would be no need to show a trench by the language of the claims at present.

Wu et al. is not relied upon to show an overhang, as one is already present in Bryant, and thus claim 12 stands rejected as in the prior Office Action.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Grant Withers/

GW

06/15/2008

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